

- L21: (3) 6392275.URPN.
- L94: (26) slanted adj sidewall and "MOS"
- L95: (31) (US-5751054-S or US-5852314-S or US-6252275)
- L96: (24) 94 not 95
- L97: (84) (slants4 adj (sidewall or (side adj wall)))
- L98: (0) 84 not (94 95)
- L99: (62) 97 not (94 95)
- L100: (29) 99 and ("MOS" or "DMOS" or memory)

Failed

Saved

(9) Lee-suk-kyun.in.

- (27) gate with (slants4 adj2 (sidewall or (side adj w
- (26) (gate with (slants4 adj2 (sidewall or (side adj
- (18) ((gate with (slants4 adj2 (sidewall or (side adj
- (16) (((gate with (slants4 adj2 (sidewall or (side ac
- (2) (((gate with (slants4 adj2 (sidewall or (side ac
- (14) (((gate with (slants4 adj2 (sidewall or (side a
- (12) ((gate with (slants4 adj2 (sidewall or (side adj

Search | Help | Browse | Queue | Clear

Default operator: OR

USPAT, US-PGPUB, EPO, IPO, IBM, TDB

P: Blinks  
P: Highlight all hit terms initially

99 and ("MOS" or "DMOS" or memory)

U	I	E	PT	P	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R	Inventor	S	C
1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 20020000380 A1	20020103	43	METHOD, CHEMISTRY, AND APPARATUS FOR NOBLE METAL ELECTROPLATING ON A MICROELECTRONIC WORKPIECE	205/102	204/212; 204/222; 204/224R;	<input checked="" type="checkbox"/>	GRAHAM, LYNDON W. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020052098 A1	20020502	16	Method of fabricating gate	438/585	257/E21.578; 438/637; 438/640;	<input checked="" type="checkbox"/>	Chang, Ching-Yu	<input checked="" type="checkbox"/>	<input type="checkbox"/>
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 20020063275 A1	20020530	19	Method of forming transistor gate	257/315	257/317; 257/E21.209; 257/E29.129;	<input checked="" type="checkbox"/>	Chang, Ching-Yu	<input checked="" type="checkbox"/>	<input type="checkbox"/>
4	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020121657 A1	20020905	25	Double-bit non-volatile memory structure and corresponding method of manufacture	257/296	257/202; 257/390; 257/401;	<input checked="" type="checkbox"/>	Chen, Chin-Yang	<input checked="" type="checkbox"/>	<input type="checkbox"/>
5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 20020142547 A1	20021003	16	Method of fabricating gate	438/257	257/315; 257/330; 257/E21.578;	<input checked="" type="checkbox"/>	Chang, Ching-Yu	<input checked="" type="checkbox"/>	<input type="checkbox"/>
6	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020177285 A1	20021128	16	Semiconductor power component and a corresponding manufacturing method	438/309	257/E21.383; 257/E29.066; 257/E29.198	<input checked="" type="checkbox"/>	Feiler, Wolfgang et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 20030020928 A1	20030130	85	Methods and apparatus for processing microelectronic workpieces using metrology	356/630		<input checked="" type="checkbox"/>	Ritzdorf, Thomas L. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>
8	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 20030130 A1	20030130	25	Double-bit non-volatile memory	438/257	257/E21.682; 257/E29.102	<input checked="" type="checkbox"/>	Chen, Chin-Yang	<input checked="" type="checkbox"/>	<input type="checkbox"/>